



09/773,872

IR-2300 (2-3077) *cgc*

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of

Richard Bullock

Date: May 13, 2005

Patent No.: 6,887,743 *B2*

Issue Date: May 3, 2005

For: METHOD OF FABRICATING A GATE DIELECTRIC LAYER FOR A THIN FILM  
TRANSISTOR

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Certificate**  
**MAY 20 2005**

**REQUEST FOR CERTIFICATE OF CORRECTION** of Correction

Sir:

Pursuant to 37 C.F.R. § 1.322(a), it is requested that the above-identified patent be corrected as follows:

Item (75) Inventors should read:

Richard Bullock, Newport (GB);  
David Paul Jones, Cardiff (GB)

A Certificate of Correction (Form PTO/SB/44) is also enclosed.

A copy of the filing receipt is enclosed showing the correct city of the first named inventor.

As this error appears to be the fault of the Patent Office, no fee is enclosed. Should any fee be required to issue the Certificate of Correction, the same may be charged to our Deposit Account No. 15-0700.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450, on May 13, 2005:

Kourosh Salehi  
Name of applicant, assignee or  
Registered Representative

Signature  
May 13, 2005  
Date of Signature

Respectfully submitted,

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SHW/KS:fs

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MAY 24 2005

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(Also Form PTO-1050)

## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. 6,887,743 B2

DATED :May 3, 2005

INVENTOR(S) :Richard BULLOCK and David Paul JONES

It is certified that error appears in the above identified patent and that said Letters Patent is hereby corrected as shown below.

**On the title page, Item (75), change the first Inventor to:**

—Richard Bullock, Newport (GB)—

MAILING ADDRESS OF SENDER:

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New York, NY 10036-8403

PATENT NO. 6,887,743

→ 0

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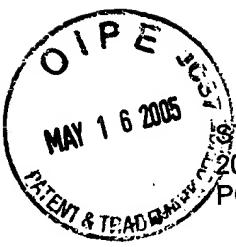
MAY 24 2005



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| APPLICATION NUMBER | FILING DATE | GRP ART UNIT | FIL FEE REC'D | ATTY.DOCKET.NO | DRAWINGS | TOT CLAIMS | IND CLAIMS |
|--------------------|-------------|--------------|---------------|----------------|----------|------------|------------|
| 09/773,872         | 02/02/2001  | 2812         | 710           | ESM00-001      | 3        | 19         | 3          |



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CONFIRMATION NO. 7976

FILING RECEIPT



\*OC00000005911338\*

Date Mailed: 03/28/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the PTO processes the reply to the Notice, the PTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Richard Bullock, Newport, UNITED KINGDOM;  
David Paul Jones, St. Fagans, UNITED KINGDOM;

Assignment For Published Patent Application

ESM Limited,;

Continuing Data as Claimed by Applicant

Foreign Applications

UNITED KINGDOM 0100216.1 01/05/2001

If Required, Foreign Filing License Granted 03/27/2001

Projected Publication Date: 07/11/2002

Non-Publication Request: No

Early Publication Request: No

Title

Method of fabricating a gate dielectric layer for a thin film transistor